REMARKS

Claim Objections

The Examiner has objected to claim 11 recited below because claim 11 recites the limitation "selectively forming a layer of a first material having **the** first conductivity type over the surface of the recess" in lines 7-8 that lacks proper antecedent basis. The Applicant respectfully submits that "the first conductivity type" of claim 11 in lines 7-8 does not lack antecedent basis because "a first conductivity type" was introduced in line 3 of claim 11.

11. (currently amended) A method of making a junction, comprising:

a) forming a gate electrode on a surface of a substrate, the substrate being of **a first conductivity type**;

b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the gate electrode, the recess having a surface;

c) selectively forming a layer of a first material having **the first conductivity type** over the surface of the recess, and within the portion of the recess that underlies the gate electrode; and

d) selectively forming a layer of a second material having a second conductivity type over and within the portion that underlies the gate electrode.

REMARKS

Claim Rejections - 35 U.S.C. §112

The Examiner has rejected claims 11 and 13-21 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 11 has been amended to particularly point out and distinctly claim the subject matter that the Applicant regards as the invention. Claims 13-21 depend upon and incorporate the elements of claim 11 and therefore reflect the amendment of claim 11.

Claim Rejections - 35 U.S.C. §102

The Examiner has rejected claims 22-30 under 35 USC 102(b) as being anticipated by Horiuchi et al. (JP/63076481). The Applicant respectfully traverses. The independent claims 22 and 27 have been amended to include the allowable limitations of independent claim 11. In particular, claim 22 has been amended to claim: "**in a continuous operation, back filling the recesses with doped crystalline material, wherein back filling comprises forming crystalline material of at least a first conductivity type within a portion of the recess partially subjacent the gate dielectric and gate electrode.**" Claim 27 has been similarly amended to claim: "**substantially filling the recess, including the portion underlying the gate electrode, with a first layer of doped crystalline material.**" Horiuchi does not teach these limitations, and in contrast teaches backfilling a region that is **not** subjacent or underlying the gate electrode or gate dielectric with a doped material, as illustrated in Horiuchi's figure 3D. In figure 3D Horiuchi illustrates the backfilled source drain regions 9, 91, 10, and 101 containing doped material. The regions 72 of Horiuchi's figure 3D that do underlie the gate electrode are insulator regions and not a doped crystalline material. Therefore, the Applicant respectfully submits that the independent claims 22 and 27, and the claims 23-26 and 28-30 that depend upon and incorporate the elements of claims 22 and 27, respectively, are not anticipated by Horiuchi and are in condition for allowance.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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